Asymmetrical Subranging R2R DAC in ULP

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Abstract – **An 8-bit R2R DAC structure is derived that is able to produce 255 steps over any subrange of the normal R2R reference voltage with the subranging being achieved without the use of active attenuators having to be added to an R2R structure. The center of the range is not restricted to the midpoint of the reference voltage level. An example is given with an application in the ULP process. The DAC reference range is .5 volts, which is the same as the VDD for the ULP process. An example DAC with a range of .25 volts to .4 volts is given.**

1. Introduction

CMOS DAC's have commonly been done by switching CMOS current sources on or off into a common node [1]. The current sources are weighted by using device widths that increase as a power of two for increasing binary-valued current sources that are turned on by the corresponding binary bit in the input word. The common output node can be used directly. In that case the DAC is a current DAC. Or the output node can drive an opamp with a resistive feedback element. In that case the output is taken on the output node of the opamp and is a voltage. A simple block diagram of an eight-bit DAC is shown in Figure 1.

Ultra Low Power (ULP) structures use CMOS devices at very low voltages. A VDD of .5 volts is typical for ULP designs. These devices tend to have higher static current leakages than regular CMOS devices that are designed to operate at 2 volts or higher. These static leakages could corrupt the current conversion process if used in the DAC structure. The output of the DAC in Figure 1 is given by equation (1). The eight-bit digital word is given by the coefficients d_i and the value is found by multiplying the coefficient d_i (0 or 1) by its corresponding column value of 2^i and then adding all the non-zero column values.

$$Vout = Vref \cdot D/2^8 = ref \cdot (d_7 \cdot 2^7 + d_6 \cdot 2^6 + \ldots + d_1 \cdot 2^1 + d_0)/2^8 = Vref \cdot (d_7 \cdot 2^{-1} + d_6 \cdot 2^{-2} + \ldots + d_1 \cdot 2^{-7} + d_0 \cdot 2^{-8}) \quad (1)$$

If Vref is assumed to be VDD, the DAC output will range from 0 volts to VDD·(255/266), depending on the value of the digital word $D = d_7 d_6 \ldots d_1 d_0$.

2. R2R DAC's

The R2R structure has been used to create Digital-to-Analog Converters (DAC's) in the lower resolution range (up to ten bits) for years [1 - 5]. The typical structure is shown in Figure 2. The R2R resistive network is used as a binary controlled current source

that injects current into the virtual-ground node of an opamp which is then forced through the feedback resistor to give an output voltage. A few of the drawbacks of this structure are the necessity of generating a low-offset gain element (opamp) as well as requiring a negative output voltage range. The output range limits are specified by the Vref and Ground voltages, as well as the feedback resistor value. The output voltage of the DAC in Figure 2 can be found from the product of the current forced into the virtual ground node of the opamp and the feedback resistor [4].

$$Vout = -2R \cdot I_{TOT} \qquad (2)$$

Where I_{TOT} is the total current from the R2R structure into the virtual ground node. With the switches as shown in Figure 2, and noting that the switches terminate at Ground in either of their positions, the output could then be found by noting that each node in the R2R structure is one-half the value of the node to the left, as given in equation (3).

$$Vout = -2R \cdot Vref \cdot (0 \cdot .5 + 1 \cdot .25 + 1 \cdot .125)/2R = -.375 \cdot Vref \qquad (3)$$

Both positive and negative supplies are needed for this type of R2R DAC structure.

3. R2R Voltage Output Structure

The R2R structure itself can be analyzed in a voltage mode to provide a voltage output directly [6]. Figure 3 shows the Thevenin equivalent structure that results from decomposing the switches and the rails they tie to. The first Thevenin equivalent circuit can be calculated from inspection. The Thevenin voltage,Vthx, is generated from the two leftmost "2R" resistors and the voltage switch between zero volts and Vref. The coefficient d_0 accounts for the switch S0 being tied to Ground or Vref. If S0 is tied to Ground d_0 equals zero, otherwise it is equal to "1". Vthx is then given by equation (4).

$$Vthx = d_0 \cdot Vref/2. \qquad (4)$$

Similarly, the Thevenin voltage Vthy can be found by combining the voltage from S1 and the Thevenin voltage Vthx. Simple analysis gives the result in equation (5).

$$Vthy = Vref \cdot (d_0/4 + d_1/2), \qquad (5)$$

Where d0 and d1 are the coefficients controlled by S0 and S1 respectively ("zero" if tied to Ground and "one" if tied to Vref). Note that if all the R2R elements are Thevenized in a network, the final Thevenin voltage would be the output voltage of the DAC that has an output impedance of R. This analysis can be extended to any number of R2R elements.For example, an eight-bit R2R voltage DAC would have its output given by equation (6)

$$Vout = Vref \cdot (d_0/256 + d_1/128 + \ldots + d_6/4 + d_7/2). \qquad (6)$$

Or, equivalently:

$$Vout = Vref \cdot (d_0 + d_1 2^1 + \ldots + d_6 2^6 + d_7 2^7)/2^8, \qquad (7)$$

which is seen to be identical to equation (1). It can be noted that the DAC range will go from Ground to $Vref(1 - 1/2^8)$ if the leftmost 2R resistor is tied to Ground (as shown in the example), or it will go from $Vref/2^8$ to Vref if the leftmost 2R resistor is returned to Vref.

4. A Subranging R2R DAC

We can modify the Thevenin equivalent sources in each of the R2R legs to provide voltages other than Ground and Vref (or VDD) by using resistor voltage dividers and switching each side of the resulting divider. A single element of the R2R structure is shown in figure (4). The switching elements are logic values provided by the logic signal and its inverse. The logic values in a CMOS circuit are VDD and Ground. The resistance added by the CMOS conducting element (either a PMOS or NMOS device) adds a small amount of resistance to the 2R resistor. To keep the ratio between the 2R element and the R element equal to two, a small amount of resistance equal to a fraction of the resistance of the "on" CMOS device can be added to the R element. The PMOS and NMOS devices can be sized to give equal "on" resistances in the non-saturation mode (triode mode) of operation [5].

The RX and RY resistor values are chosen to generate the maximum and minimum voltages that will appear on the output of the DAC. The Thevenin equivalent max or min voltage is determined by the logic level (and hence voltage) of Dn. The parallel combination of RX and RY will also have to have an equivalent resistance equal to 2R.

A subranging DAC has been designed for the ULP (Ultra Low Power) process developed at the University of Idaho with the DAC output requiring 255 voltage steps between .2 volts and .3 volts. The VDD of the ULP circuit was .5 volts. Figure 5 shows the R2R schematic and Figure 6 shows the simulated output results.

An equivalent leftmost "2R" element has to be included in the resistor chain as shown in Figure 5. This divider provides a Thevenin equivalent voltage of .2 volts (the minimum voltage in the DAC range) and the parallel combination of the 50.15K and 33.48K give a 2R value of 20K. Voltage sources provide the logic and timing necessary for the simulation step output shown in Figure 6.

The glitches in the DAC output simulation are due to the transients in the switching and are not error levels in the DAC itself. The output model for this DAC would be a voltage source in series with a 10K resistor.

5. Asymmetric Subranging R2R DAC

Figure 4 shows the Thevenin equivalent of the symmetric subranging R2R structure and can be modified to give an asymmetric subrange if two separate equivalent circuits are switched in so as to be mutually exclusive. This can be accomplished if the CMOS devices are used as switches instead of logic gates. Figure 7 shows how the two 2R sections can be separately switched into the R2R ladder. The upper and lower voltages (v+ and v-) can be set arbitrarily between (or equal to) the rails but once set, have to be the same for all sections of the ladder. The resistor values are chosen from the resistor-divided requirement of providing v+ or v- as well as having to be equal to 2R when combined in parallel. Figure 8 shows an implementation of the idea using CMOS devices as "on" – "off" switches. The simulated results using v+ = .4 volts and v- = .25 volts is given in Figure 9.

Figure 10 shows the die of a chip done for an rf application that required three separate DAC's to set threshold levels on high-speed comparators. Test data has been taken and

the DAC's actually function according to the design specification. Paper submission deadlines precluded including the data in this report.

6. Conclusions

The classic R2R structure that has been used in DAC's for years has been modified to give a subranging voltage output. No active analog devices are needed to provide a usable output and the control structure consists of simple logic gates. The DAC examples used in this paper could also be used with a resistive feedback opamp to provide a selectable gain or attenuation. The opamp would also be able to operate within a single supply environment since its output would not necessarily have to go negative (below Ground) as required in the normal R2R structure. Both symmetric and asymmetric examples were given.

References

[1] R. Jacob Baker, Harry W. Li and David E. Boyce, "CMOS Circuit Design, Layout, and Simulation," IEEE Press, 1998, pp. 797 – 800.

[2] R. L. Geiger, P. E. Allen, and N. R. Strader, "VLSI – Design Techniques for Analog and Digital Circuits," McGraw-Hill Publishing Co., 1990.

[3] Razavi, Behzad, "Data Conversion Sytem Design," IEEE Press, 1995, pp. 84 – 89.

[4] Grebene, Alan B., "Bipolar and MOS Analog Integrated Circuit Design," John Wiley & Sons, 1984.

[5] Johns, David A., and Martin, Ken, "Analog Integrated Circuit Design," John Wiley & Sons, 1997, pp. 471 - 473.

[6] Cox, David F., "Symmetrical Subranging R2R DAC in ULP", Tenth NASA Symposium on VLSI Design, pp 2.1.1 – 2.1.6, March, 2002, Albuquerque, New Mexico.

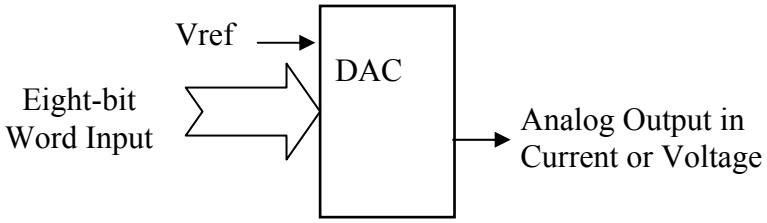

Figure 1. Simple DAC symbol.

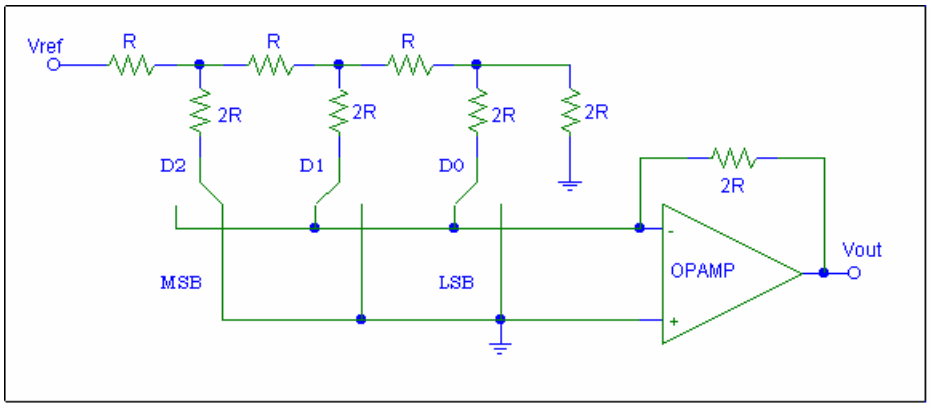

Figure 2. R2R DAC with voltage output

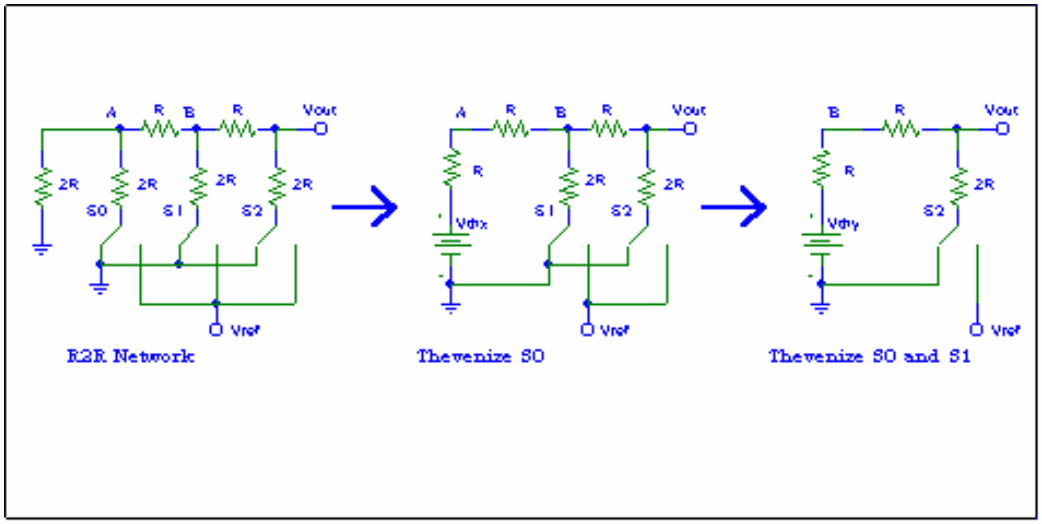

Figure 3. Steps to Thevenize R2R network.

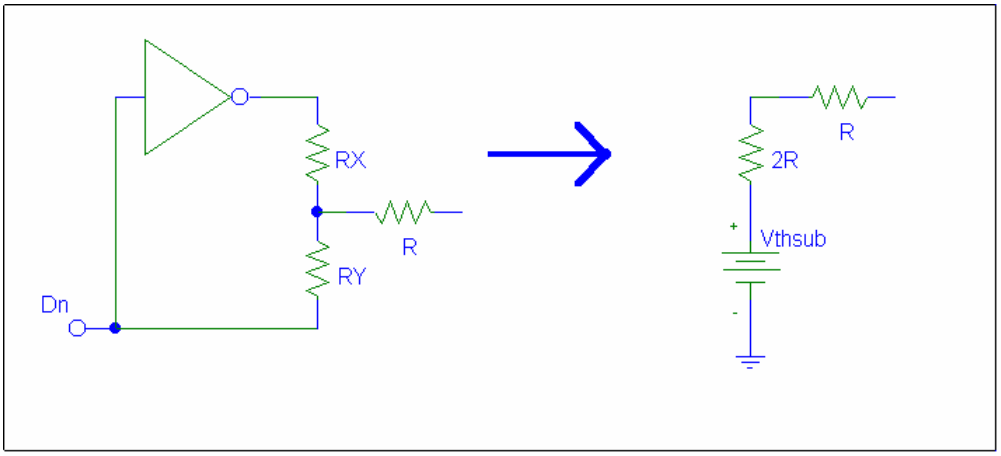

Figure 4. Means to Develop a Subranging Element in an R2R DAC.

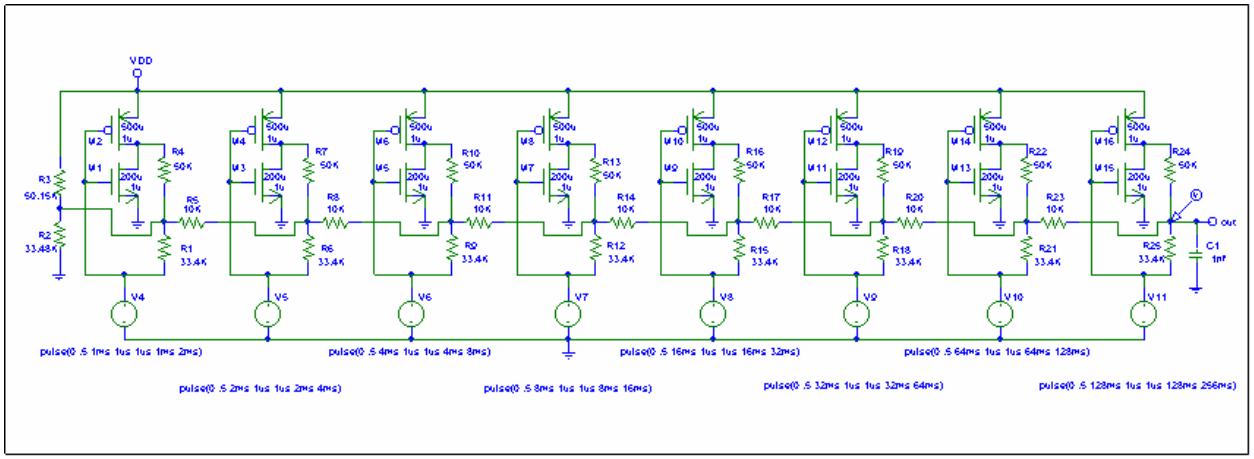

Figure 5. 8-bit R2R Subranging DAC with .1 volt range.

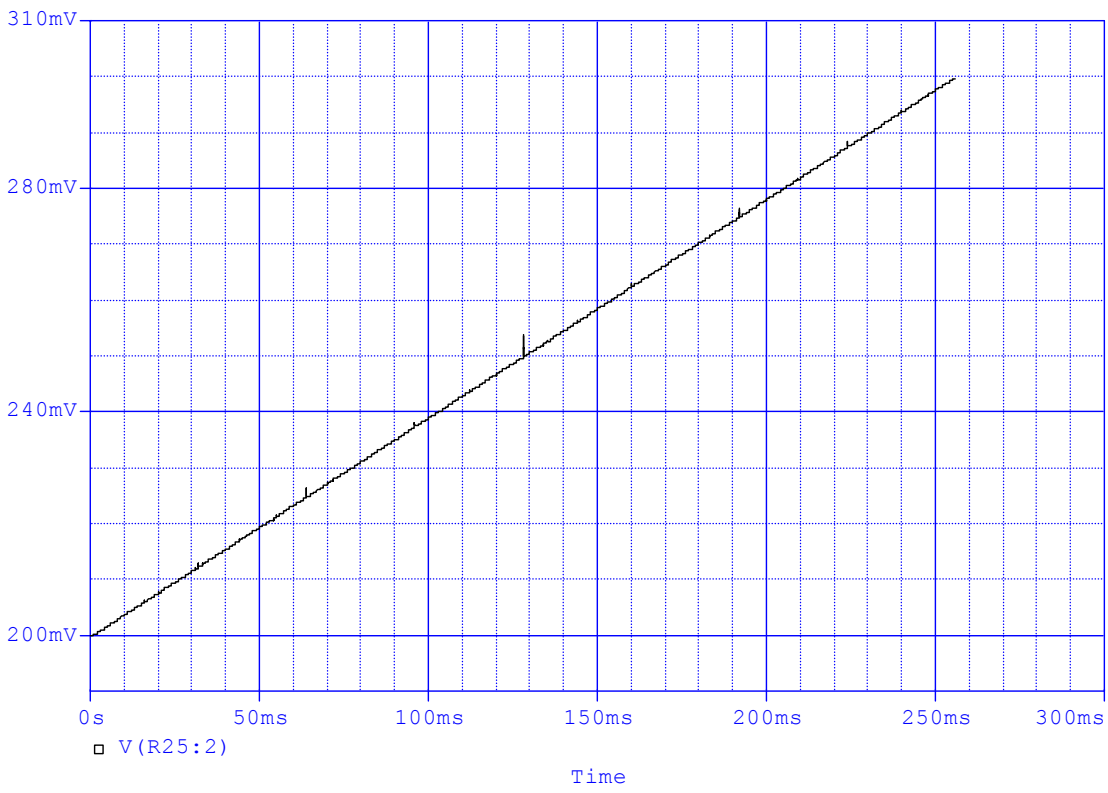

Figure 6. Symmetric Subranging R2R DAC Simulation Results.

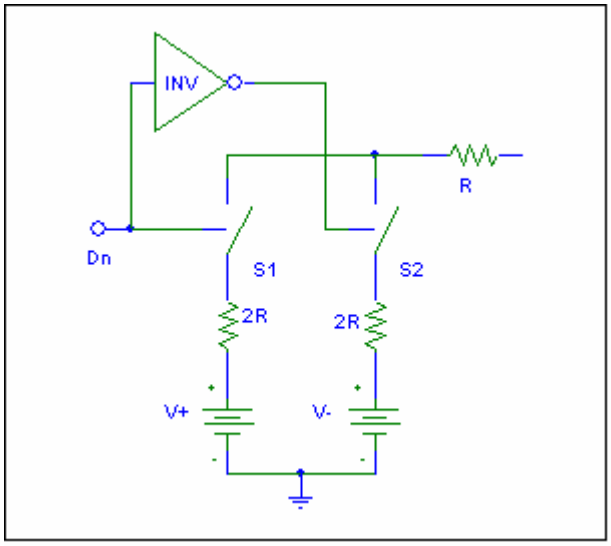

Figure 7. Asymmetric R2R DAC element.

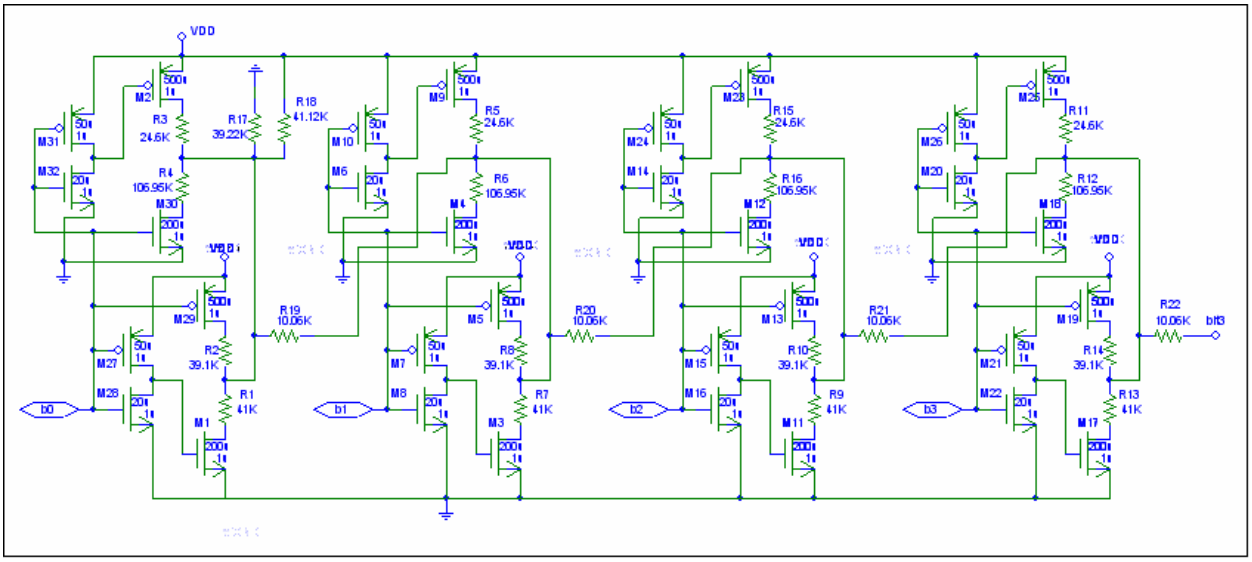

Figure 8. Four-bit Asymmetrical Subranging R2R DAC.

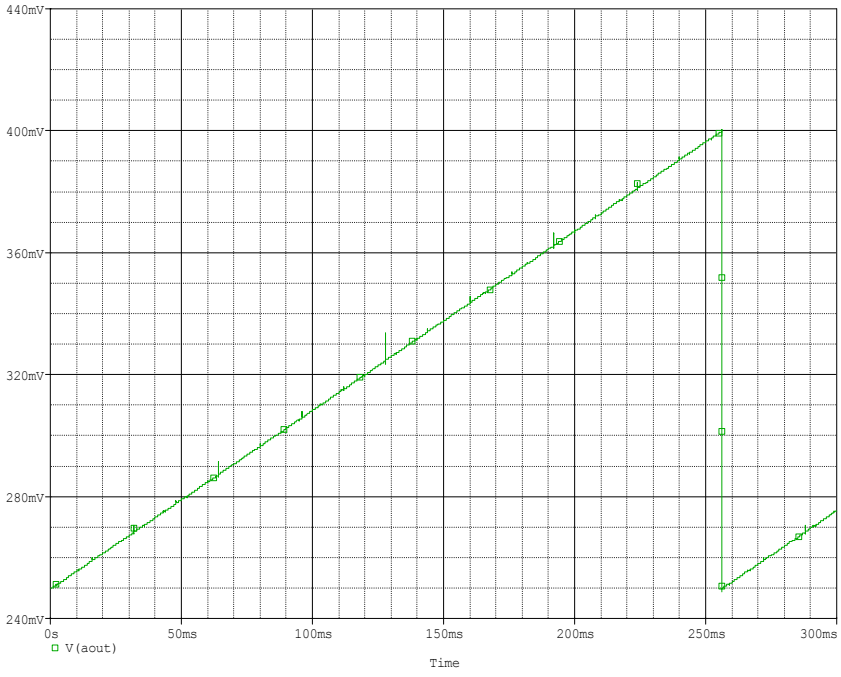

Figure 9. Asymmetrical Subranging R2R DAC simulation output.

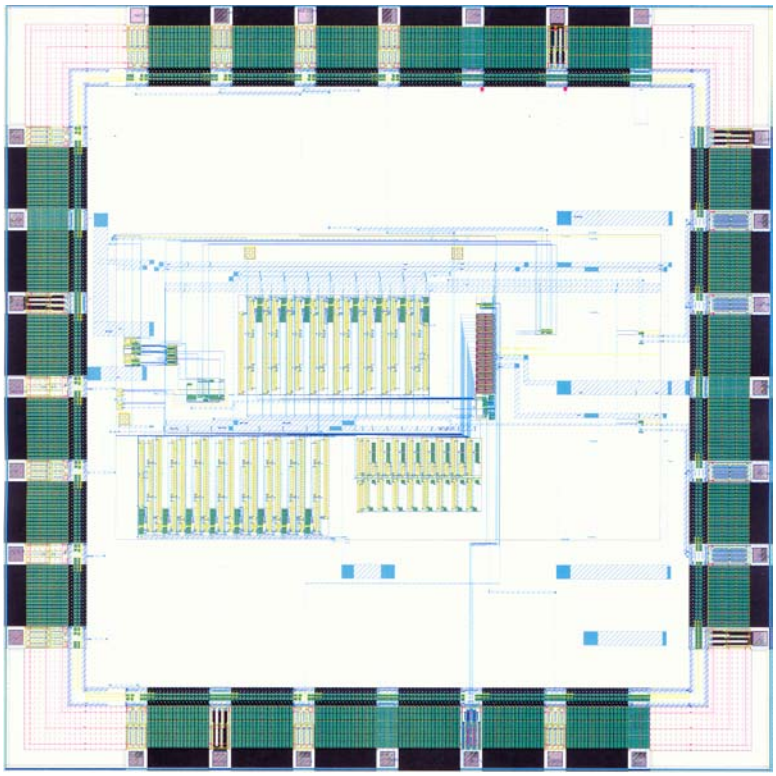

Figure 10. Digitizer Layout Using Three R2R Dacs.